TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2075 Chaitra

Exam.	Regular / Back		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic *(EX 401)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt <u>All</u> questions.*
- ✓ *The figures in the margin indicate <u>Full Marks</u>.*
- ✓ *Assume suitable data if necessary.*

1. Write down the advantages and disadvantages of digital signals over analog signals. [4]
2. Convert the following: [1.5×4]
   a) $(53.125)_{10} = (?)_2$
   b) $(615)_8 = (?)_{BCD}$
   c) $(10011)_{Gray} = (?)_8$
   d) $(11001001)_{excess\text{-}3} = (?)_8$
3. State and prove De Morgan's theorem. Design X-NOR gate using anyone of universal gate. [4+2]
4. Simplify the following expressions using K-map and also draw the logical circuit.
   $Y(A, B, C, D) = \Sigma (0, 2, 3, 4, 7, 8, 10, 13)$ and
   $d = \Sigma (5, 6, 12)$ [4+2]
5. Construct the 3-bit magnitude comparator circuit. [5]
6. Implement the following function using 8×1 MUX.
   $F (A, B, C, D) = \Sigma (0, 2, 3, 6, 7, 8, 12, 13, 15)$ [5]
7. Construct Full Adder using half Adder. [4]
8. Explain operation of S-R flip-flop with its logical diagram characteristics table, characteristics equation excitation table and timing diagram. [8]
9. Convert J-K flip flop to S-R flip flop. [6]
10. Explain the working principle of 4-bit parallel in serial out shift register with its timing diagram. [6]
11. Construct an Asynchronous Decade counter. [5]
12. Design a sequential machine that detects 101 from input stream X by making Y is 1. Using J-K flip-flop. [10]
13. What is ROM? Implement given functions $F_1 (A,B, C) = \Sigma (2, 3, 5, 6)$ and $F_2 (A, B, C) = \Sigma (0, 1, 5)$ using ROM. [1+4]
14. Draw the circuit diagram of frequency counter. [4]

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1. Differentiate between edge and level triggering system with example. [4]
2. Define Gray Code and convert $(11101)_{\text{Gray code}}$ to binary. When $(FF)_H$ is ANDed with $(CA)_H$ what will be the resulting number. [4+2]
3. Simplify $F(A, B, C, D) = \Sigma(2, 3, 6, 7, 9, 10, 11)$ and $d = \Sigma(5, 8, 12)$ using K-map. Result in SOP and POS form. [4+4]
4. Define encoder. Design 4×16 Decoder using 2×4 Decoder only. [2+4]
5. Explain 2-bit fast Adder with its logical diagram and write the advantage of fast Adder. [4+2]
6. Explain the operation of J-K flip flop with its logical diagram characteristics table, characteristics equation, excitation table and timing diagram. [8]
7. Explain the 4-bit SISO shift Register with its timing diagram. [6]
8. Design Mod-5 synchronous counter using JK flip flop. [
9. Design sequential machine that has one input x and one output z. The machine is required to give output 1 when it contains message 1101 using S-R flip flop. [1]
10. Design 12-Hr. digital clock. [5]
11. Write short notes: (Any two)
    a) Ring counter
    b) Binary parallel Adder
    c) PLA

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1. Write the basic difference between analysis and digital signals with examples. [3]
2. Perform the following code conversions. [1.5×4]

   (i) $(430.25)_8=(?)_{16}$
   (ii) $(39.75)_{10}=(?)_8$
   (iii) $(17)_{10}=(?)_{gray}$
   (iv) $(17)_{excess\text{-}3}=(?)_{BCD}$
3. a) State and prove De-Morgan's laws. [2]

   b) Realize 3 inputs XOR gates using NAND gates only. [3]
4. Define minterms and maxterms. Simplify the following using k-map and implement the result using NOR gates only. [2+4+2]

   $F(A,B,C,D) = \Sigma m (0,1,2,5,8,14) + d(4,10,13)$
5. Implement 1:16 demultiplexer using 1:2 demultiplexer. [4]
6. What is hazard? Explain types of hazards with hazard cover techniques used in K-map simplification. [1+4]
7. Define excess-3 code with examp. Design a binary to excess-3 code converter circuit using basic gates. [2+5]
8. Differentiate between combinational and sequential circuit. Explain working principle of master slave JK flip-flop. [2+4]
9. Define shift registers with its application. Explain the working principle of 4 bit Ring counter with its timing diagram. [2+5]
10. Design a 3 bit synchronous up counter where the bit combination of each states are in gray system. (Use T-flip-flop in your design.) [8]
11. Using melay circuit with J-K flip-flops design a synchronous sequence detector that produces output Z=1 when it detects the serial input X=010. [10]
12. Differentiate between RAM and ROM. Implement $F1=\Sigma(1,2,4,6)$ and $F2=\Sigma m(0,2,3)$ using PROM. [2+4]
13. What are the applications of digital devices? Explain frequency counter. [1+4]

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