TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2076 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT 603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Draw the instruction cycle state diagram with example. [6]
2. Write down the code to evaluate Y = (A - B/C)*[D + (E*G)] in three address, two address, one address and zero address instruction formats. [8]
3. Define addressing modes. Mention the different types of addressing modes and comparison between them. [2+6]
4. How address of micro instruction is generated by next address generator in control unit? Explain with suitable diagram. [8]
5. Explain four stage instruction pipeline and also draw a time-space diagram for four segments having six tasks. [10]
6. Explain the Booth's algorithm for multiplication. Multiply 10 × (-5) using Booth's multiplication algorithm. [5+5]
7. Comparison between restoring and non-restoring division algorithms with example. [6]
8. Define cache mapping techniques. Explain direct mapping technique with suitable diagram. Why replacement algorithm is necessary in associative mapping? Justify. [2+4+4]
9. Comparison between program I10, Interrupt driven I10 and direct memory access. Why data communication processor is required in an I10 organization. [8+2]
10. Discuss about hypercube interconnection network with example. [4]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2075 Chaitra

Exam.	Regular / Back		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT 603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Define computer architecture. Discuss the limitations of using single bus system to connect different devices. What does width of address bus represent in a system? [2+2+2]
2. Design an 2-bit ALU that can perform subtraction, AND, OR and XOR. [8]
3. Write a code for Y=(A+B)/C + D/(E*F) using three address, two address, one address and zero address instruction format. [8]
4. Differentiate hardwired and micro-programmed control unit. Draw and explain block diagram of micro-programmed sequencer for control memory. [10]
5. Derive expression showing speed up ratio equals number of segments in pipeline. Discuss in detail about data dependency problem that arises in pipelining along with its solution. [3+5]
6. Write an algorithm for non restoring division. Perform the 10/3 using restoring division algorithm. [3+7]
7. Multiply -6×-11 using Booths Multiplication algorithm. [6]
8. Write characteristics of memory system? Suppose main memory has 64 blocks and cache memory has 8 blocks when 10 blocks of main memory are used, show how mapping is performed in direct mapping technique. [4+6]
9. Explain three reasons behind the requirement of I/O interfaces. Why memory address spaces are reduced memory mapped I/O ? Describe DMA controller with suitable block diagram. [3+2+5]
10. Explain inter-processor synchronization with example. [4]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2076 Ashwin

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT 603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. What is PCI? Explain the design goals and performance metrics for a computer system regarding its organization and architecture. [1+5]
2. Write the arithmetic statement Y=(W+X)*(Y-Z) using Zero, One, Two and Three address instruction format. [8]
3. Explain the different types of addressing modes and compare each of them. [8]
4. Explain block diagram of micro-programmed control organization. Describe various fields in micro-instruction format with diagram showing different fields. [4+6]
5. Describe the hazard in a pipeline. Explain the different types of hazards. How can these be overcome? [2+4+2]
6. Write an algorithm of booth multiplication. Perform 8×4 using booth multiplication algorithm. [10]
7. Differentiate between restoring division and non-restoring division and non-restoring division algorithm. [6]
8. Describe cache operation in briefly. Explain about associative mapping technique. Give reasons why replacement algorithm is not required in direct mapping technique. [2+6+2]
9. Explain the DMA operation with block diagram. How does DMA have request over the CPU when both request a memory transfer? [8+2]
10. Discuss about tightly-coupled multiprocessor with block diagram. [4]

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36 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2074 Ashwin

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Explain instruction cycle state diagram with interrupt. [6]
2. Write codes using 3, 2, 1 and 0 address instruction formats to perform given operation. [8]

   $X = (A*B/C) - (D+E/F)$
3. Describe various fields in microinstruction format. Explain about the sequencing techniques used in microinstruction format with necessary diagram. [10]
4. Explain microinstruction format showing all the fields in detail. Write symbolic microprogram for fetch cycle. [10]
5. Explain arithmetic pipeline with an example of 4 segments. Describe different types of array processing. [6+4]
6. Write an algorithm flow chart and hard ware design of restoring division with example. [10]
7. Draw a flow chart for floating point multiplication algorithm. [4]
8. Explain about associative mapping technique. Give reasons why replacement algorithm is required in associative mapping technique? [8]
9. Explain the block diagram of DMA controller and also explain how DMA is used to transfer data from peripheral. [10]
10. Differentiate between tightly coupled multiprocessors and loosely coupled multiprocessors. [4]

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36 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2073 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Explain instruction cycle state diagram with interrupt. [6]
2. Write a code for Y = A/(B+C) + (D+E)*F using three address, two address, one address and zero address instruction format. [8]
3. Explain different types of data manipulation instructions with examples. [10]
4. Why is micro-programmed control unit more flexible as compared to hardwired control unit? Explain the sequencing technique used in control memory. [10]
5. Explain the function of four segment pipeline and also draw a space diagram for four segment pipeline with example. [10]
6. Write an algorithm for division of floating point number. [4]
7. Explain Booth algorithm of multiplication with hardware implementation diagram and multiply-10×6. [10]
8. Explain major characteristics of memory. Explain LRUC (Least Recently Used) replacement policy with example. [8]
9. Why I/O processor is necessary in an input-output organization? Explain about DMA control with necessary diagram. [10]
10. Design for 4×4 omega switching network and show the switch setting required to connect input 3 to output 1. [4]

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36 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2073 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Explain instruction cycle state diagram with interrupt. [6]
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8. Explain major characteristics of memory. Explain LRUC (Least Recently Used) replacement policy with example. [8]
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10. Design for 4×4 omega switching network and show the switch setting required to connect input 3 to output 1. [4]

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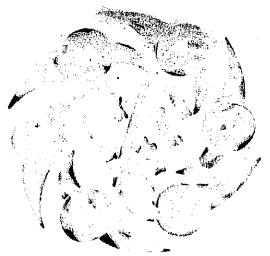

36 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2074 Ashwin

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Explain instruction cycle state diagram with interrupt. [6]
2. Write codes using 3, 2, 1 and 0 address instruction formats to perform given operation. [8]
   $X = (A*B/C) - (D+E/F)$
3. Describe various fields in microinstruction format. Explain about the sequencing techniques used in microinstruction format with necessary diagram. [10]
4. Explain microinstruction format showing all the fields in detail. Write symbolic microprogram for fetch cycle. [10]
5. Explain arithmetic pipeline with an example of 4 segments. Describe different types of array processing. [6+4]
6. Write an algorithm flow chart and hard ware design of restoring division with example. [10]
7. Draw a flow chart for floating point multiplication algorithm. [4]
8. Explain about associative mapping technique. Give reasons why replacement algorithm is required in associative mapping technique? [8]
9. Explain the block diagram of DMA controller and also explain how DMA is used to transfer data from peripheral. [10]
10. Differentiate between tightly coupled multiprocessors and loosely coupled multiprocessors. [4]

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01/08

36 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2072 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Define computer architecture and computer organization. How can we maintain a performance balance between processor and memory? Discuss the limitations of using single bus system to connect different devices in any given system. [2+2+2]
2. What do you mean by instruction format? Write codes for given operation using 3-,2-,1- and 0- address instruction format. [4+8]

   X=(A-B*F)*C+D/E
3. Differentiate between RISC and CISC. [6]
4. What factors cause micro-programmed control unit to be selected over hardwired control unit. Explain with relevant block diagram, how address of control memory is selected in micro-programmed control unit. [3+7]
5. Describe Flynn's classification. Explain control pipeline hazard and its solutions. [4+6]
6. Explain Booth's multiplication hardware algorithm with diagram. Multiply -5×-9 using Booth's multiplication algorithm. [5+5]
7. Draw the flowchart for division of floating point numbers. [4]
8. Draw the memory hierarchy. Explain direct cache mapping with its merits and demerits. [2+6]
9. Differentiate between Isolated I/O and Memory-mapped I/O. Describe DMA controller with suitable block diagram. [4+6]
10. Discuss about inter process synchronization with the suitable mechanism? [4]

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37 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2073 Shrawan

Exam.	New Back (2066 & Later Batch)		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. What do you mean by interconnection structure? Explain different types of interconnections indeed required in Computer Architecture. [2+4]
2. Write a code for $Y = A*(B+D/C)+(G*E)/F$ using three addresses, two address, one address and zero address instruction format. [8]
3. Following instructions are given: [10]

   i) LDA 2000H
   ii) MVI B, 32H
   iii) STAX D
   iv) MOV A, B

   Which addressing modes are used in the above instructions? Explain briefly about them.
4. Explain microinstruction format used in microprogramming Control unit and write micro program for fetch cycle. [6+4]
5. Explain in detail how the arithmetic pipeline increases the performance of a system. [7]
6. "RISC has the ability to use efficient instruction pipeline". Justify the statement. [3]
7. Explain signed binary division algorithm. Use the non-restoring division algorithm to devide 15 by 4. [8]
8. Explain floating point addition and subtraction algorithm with example. [6]
9. Describe how set associative mapping combines the feature of direct and associated mapping technique. Explain different write policy techniques in cache memory. [5+3]
10. Why input-output processor is needed in an input-output organization? How does a computer know which device issued the interrupt; if multiple devices, how does the selection take place? [5+5]
11. Describe how the multiprocessor systems increase the performance level and reliability. [4]

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01 / 10

36 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2071 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. What are the major differences between computer architecture and computer organization? What does the width of data bus and address bus represent in a system? Why is bus hierarchy required? [2+2+2]
2. Explain the general organization of register in CPU. Describe the operation of LD (load) instruction under various addressing modes with syntax. [6+4]
3. What are the different types of instructions? How can you perform X = (A+B) × (C+D) operation by using zero, one, two and three address instruction format. Assume A, B, C, D, X are memory address. [3+5]
4. What is address sequencing? Explain the selection of address for control memory with its block diagram. [3+7]
5. Explain the Arithmetic pipeline and instruction pipeline with example. [10]
6. Draw the flowchart for floating point Division. [4]
7. Design a booth multiplication algorithm hardware. Multiply 5 and -6 using booth multiplication algorithm. [4+4]
8. Explain cache organization. Explain the cache mapping techniques with example. [4+6]
9. Highlight the role of I/O interface in a computer system. Describe the drawbacks of programmed I/O and interrupt driven I/O and explain how DMA overcomes their drawbacks. [4+6]
10. How can multiprocessor be classified according to their memory organization? Explain. [4]

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36 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2072 Kartik

Exam.	New Back (2066 & Later Batch)		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Differentiate between computer architecture and computer organization. Explain the computer functions with different cycles. [3+3]
2. Write a code for Y = (A+B)*(C+D)+G/E*F using three address, two address one address and zero address instruction format. [8]
3. Mention the different types of addressing mode and compare each other. [10]
4. Explain the address sequencer with the help of a block diagram. Explain about microinstruction format in detail. [5+5]
5. Define pipeline and explain its types. Describe different pipeline hazards with example. [4+6]
6. Draw the flowchart for restoring division method. [4]
7. Explain Booth multiplication algorithm. Multiply -6×12 using Booths algorithm. [4+6]
8. Draw the memory hierarchy. Explain Associative Cache Mapping with example. [2+6]
9. What are the different types of priority interrupt? Explain the communication between CPU and IOP with necessary block diagram. [4+6]
10. Explain about multiprocessor and multiprocessing in brief. [4]

01/10

36 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2070 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Explain the interconnection of CPU with Memory and I/O devices along with different operations over them. [3+3]
2. Write down the Y = A/B+(C×D) + F(H/G) equation in three address, two address, one address and zero address instruction. [8]
3. Mention the different types of addressing modes. Compare each of them with algorithm as well as advantages and disadvantages. [10]
4. Differentiate between hardwired and micro-programmed control unit. How does a sequencing logic work in micro-programmed control unit to execute a micro-program? [4+6]
5. Explain the arithmetic pipeline and instruction pipeline with example. [10]
6. Explain the non-restoring division along with its algorithm, flowchart and example. [8]
7. Explain the Booth algorithm and multiply Y = 8×9 using Booth algorithms. [6]
8. Mention the 'characteristics of computer memory. Differentiate between associative mappings and set associative mapping with example. [3+5]
9. How does DMA overcome the problems of programmed I/O and interrupt-driven I/O techniques? Explain. [5]
10. Why IOP is use in I/O organization? Explain. [5]
11. Explain the characteristics of multiprocessors. [4]

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37 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2071 Shawan

Exam.	New Back (2066 & Later Batch)		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. What do you understand by Bus Interconnection? What are the driving factors behind the need to design for performance? [2+4]

2. Explain Instruction Format with its types? Illustrate the code to evaluate to evaluate: Y = (A+B) * (C+D) using three address, two address, one address and zero address instruction formats. [2+6]

3. Describe the instruction cycle state diagram? Design a 2-Bit ALU that can perform addition, AND, OR operations. [3+3]

4. Explain the organization of a control memory. Discuss the microinstruction format with the help of a suitable example. [4+6]

5. Discuss about parallel processing? How parallel processing can be achieved in pipelining, explain it with time-space diagram for four segments pipeline having six tasks. [4+6]

6. Write down the detail algorithm of Booth Multiplication. Illustrate the multiplication of (9) and (-3) using 2's complement method. [5+5]

7. What is Memory Hierarchy and why it is formed in computer system? Explain the Direct cache memory mapping technique using organization diagram and appropriate example. [2+6]

8. What are the functions of I/O Module? What is the purpose of priority interrupt; explain priority interrupt types with key characteristics. [3+7]

9. Differentiate the following [4x3]

   a. RISC and CISC
   b. Restoring and Non-Restoring Division
   c. Crossbar Switch and Multistage Switching Network

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37 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2070 Ashad

Exam.	New Back (2066 & Later Batch)		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. What is performance balance and why is it required? Explain different elements of bus design. [6]
2. Define the addressing mode and explain the different types of addressing modes with example. [10]
3. What are the stages of ALU design? Explain with the example of 2-bit ALU performing addition, subtraction, OR and XOR. [8]
4. What are the differences between hardwired implementation and micro-programmed implementation of control unit? Explain with steps involved when you are designing micro-program control unit. [4+6]
5. What is instruction hazard in pipeline? What is the four segment instruction pipeline? Explain with example. [2+8]
6. How division operation can be performed? Explain with its hardware implementation. [10]
7. Draw a flowchart of floating point subtraction. [4]
8. What are the major differences between different cache mapping techniques? Suppose main memory has 32 blocks and Cache memory has 8 blocks when 10 blocks of main memory are used, show how mapping is performed in direct mapping technique. [6+2]
9. Differentiate between programmed I/O, interrupt-driven I/O and direct memory access (DMA). [10]
10. Explain the interprocessor synchronization with example. [4]

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37 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2069 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Differentiate between computer organization and architecture. What do you mean by bus interconnection? [3+3]
2. What are the different types of instruction formats? Explain with example. [10]
3. Define data manipulation instruction. Explain the logical and bit manipulation instruction with mnemonic code. [3+5]
4. What is address sequencing in control unit? Explain with necessary figure. [10]
5. What is vector processing? How pipelining improves the performance of a computer? Explain with example. [10]
6. Explain the restoring division algorithm and hardware design with example. [10]
7. Draw the flowchart of floating point multiplication. [4]
8. What is cache memory? What are the different ways the cache can be mapped? Explain with example. [2+6]
9. What are the functions of I/O Module? Why priority interrupt is needed for data transmission between CPU and I/O device. Explain the types of priority interrupt in detail. [10]
10. Compare and contrast the interconnection structures used in multiprocessing environment. [4]

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37 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2069 Ashad

Exam.	New Back (2066 & Later Batch)		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT 603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Explain bus hierarchy and why it is required. Describe method of bus arbitration. [6]
2. Write down the code to evaluate Y=AB+(C/D)+E(F/G) in three address, two address, one address and zero address instruction format. [8]
3. Compare RISC and CISC architecture. [5]
4. What do you mean by data manipulation instruction? Explain the logical and bit manipulation instruction with mnemonics code. [5]
5. Design microinstruction format, symbolic and binary micro program that can perform fetch cycle, indirect cycle and add operation. Also design and describe sequencing technique that is used in control unit. [10]
6. What is arithmetic pipelining? Explain with example. [6]
7. How can we increase the performance of a computer by adopting vector computation? [4]
8. Describe floating point addition and subtraction flow chart. [6]
9. How division of signed integers can be performed? Explain with example. [8]
10. What do you mean by mapping function? Why replacement algorithm is used in associative and set associative mapping? Explain with example. [2+6]
11. Describe interrupt driven I/O. Compare interrupt driven I/O with programmed I/O. Explain how data transfer is performed with direct memory access (DMA). [3+3+4]
12. Discuss the difference between tightly coupled multiprocessor and loosely coupled multiprocessors? [4]

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36 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2068 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: -Computer Organization and Architecture *(CT 603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Explain the functional view and four types of operations used in computer. [6]
2. What are most common fields in an instruction? How can you perform X=(E+F)*(G+H) operation by using zero, one, two and three address instruction format. Assume that E, F, G, H and X are memory addresses. [8]
3. Define addressing mode. Explain different types of addressing modes with example. [10]
4. Explain various fields in micro-instruction format with neat and clean block diagram. Describe how address of control memory is selected. [3+7]
5. What are the hazards in instruction pipelining? How can they be resolved? Explain. [10]
6. Explain Booth algorithm. Use the Booth algorithm to multiply 23(multiplicand) by –21(multiplier), where each number is represented using 6 bits. [8]
7. Explain floating point division algorithm. [6]
8. Explain cache read operation. What are the demerits of direct mapping technique used in cache design and describe in details any one of the mapping technique that solves these problems. [8]
9. Why input-output processor is needed in an input-output organization? Explain with block diagram. [10]
10. Define the multiprocessor and its characteristics. [4]

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