TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2076 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEL,BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX 502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Explain Gray code with suitable examples. [3]
2. State and prove the De-margin's theorem and perform the addition (-47+27) by using 2' complement method. [3+3]
3. Simplify the function using K-map F=Σ (1,2,3,8,9,10,11,14) and D = Σ (0,4,12). Also realize the simplified circuit using NAND Gates. [4+2]
4. Describe the importance of parity bits in communication system. Explain 3 bits even parity generator circuit clearly. [2+4]
5. Realize a full subtractor circuit by combining only one 1:4 demultiplexer and standard gates. [5]
6. Explain the operation of 8:1 multiplexer with necessary diagrams. Construct 32:1 MUX using only 8:1 MUXs. [3+3]
7. Explain the serial in parallel-out (SIPO) shift register with timing diagram of 1101 data input. [6]
8. Explain the operation of edge triggered J-K Flip-Flop with necessary diagram and excitation table. [6]
9. Differentiate between combinational and sequential logic circuits. Construct and explain mod-12 asynchronous down counter with negative edge clock triggering system. Use JK flip-flops and necessary logic gates. [2+6]
10. Design the synchronous decade counter using T flip-flop and also show its timing diagram. [8]
11. Explain the operation of TTL two input OR gate with schematic diagram and also define the propagation delay time and power dissipation. [4+2]
12. With the help of block diagram, explain the operation of digital frequency counter. [4]
13. Consider a sequential detector that receives binary data stream at its input 'X' and signals when a serial sequence '1011' arrives at the input by making its output'Y' high, otherwise output remains low. Design a sequence detector state machine using positive edge triggered T flip flops. [10]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2075 Chaitra

Exam.	Regular / Back		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX 502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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1. a) Explain excess-3 code with suitable examples. [2.5]
   b) Define combinational logic circuit. [2.5]
2. Simplify the function using K-map $F=\sum(0,1,4,8,10,11,12)$ and $D=\sum(2,3,6,9,15)$. Also convert the result into only NAND gates. [6]
3. Design the operation of octal priority encoder with neat diagram. [7]
4. Design a simplest logic circuit for 'b' segment of the BCD-to-7 segment display decoder. [6]
5. Explain the operation of JK flip flop showing its logic diagram, characteristic table and then derive its characteristic equation and excitation table. [6]
6. Draw a 4 bit PISO shift register and explain its operation along with timing waveform with 1101 data load in input. [6]
7. Explain the working principle of 4 bit down asynchronous counter with neat timing diagram using negative clock edge triggering. [6]
8. Design a mod-6 synchronous counter using T Flip-Flops with timing diagrams. [7]
9. Describe the voltage profile of TTL. Explain the working principle of tristate TTL inverter. [2+6]
10. Design a synchronous sequential machine such that it gives output Z=1 if input contains the sequence of message 011 and it retains in its own state in other condition giving output zero. Use RS-Flip-Flop. [11]
11. Draw the circuit diagram of 3 input CMOS gate and explain its operation. [6]
12. Illustrate time measurement circuit with block diagram. [6]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2076 Ashwin

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX 502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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1. a) What is a gray code? Compare with binary numbers. [3]
   b) List the advantages of digital signal over analog signal. [3]
2. Describe De' Morgan's laws with examples. Construct XOR gate using only 3-inputs NAND gates. [2+3]
3. What is a decoder? Realize a 2-to-4 line decoder as a full adder circuit. [1+5]
4. Simplify the following function using K-map. And also draw reduced circuit using NOR gate y(A, B, C, D) = ΠM (0,2,3,8,10,11,12,15) and d=ΠM(7,13,14). [5+2]
5. a) Explain the operation of two 4-bit parallel adder with neat diagram. [5]
   b) Realize the logic circuit of 1×16 DMUX using 1×4 DMUX and gates if necessary. [3]
6. Differentiate between combination and sequential circuit. Explain briefly how latch can be used as bounce eliminator. [2+4]
7. Explain how 1001 data can be stored and retrieve n PISO shift register with neat diagram and truth table. [7]
8. Construct a mod-12 asynchronous up counter with positive clock edge triggering Implement only T flip-flops. [5]
9. Design BCD synchronous counter with circuit diagram, truth table and timing waveform. Use T flip-flop. [7]
10. Draw the schematic diagram of 2-input TTL NAND gate and explain about CMOS characteristics. [4+2]
11. Design a sequential machine with one input x and one output z which gives output z=1 when serial input containts 1011 message. Use J-K flip-flop. [12]
12. With the help of block diagram explain the operation of frequency counter. [5]

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17 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2074 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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1. a) Define TTL IC Signal levels for Input and Output logic with example. [3]
   b) Convert 37.432 decimal number to binary. [3]
2. a) State and prove De-Morgan's theorems with necessary diagrams. Prove that negative logic OR Gate is equivalent to positive logic AND Gate. [4+2]
   b) What is Gray code? Explain with example. [2]
3. a) Minize the expression and implement the reduced expression by using NAND gates.
   $F = \overline{A}B\overline{C}\overline{D} + \overline{A}B\overline{C}D + \overline{A}BCD + \overline{A}BC\overline{D} + A\overline{B}\overline{C}\overline{D} + A\overline{B}\overline{C}D + A\overline{B}C\overline{D} + AB\overline{C}\overline{D} + ABC\overline{D}$ [4+2]
   b) What do you mean by Max term? Explain with example. [3]
4. Design the 32:1 Multiplexer using 4:1 multiplexers tree concept and implement the function $F = \sum(0,1,3,8,9,13)$ using suitable Multiplexer. [4+2]
5. a) Explain the operation of 3 bit magnitude comparator with truth table and draw the circuit. [5]
   b) Draw the circuit to add following bits 1011 and 1100. [3]
6. a) Write down the drawback of SR Flip-Flop. Explain the operation of edge triggered JK Flip-Flop with timing diagram and truth table. [2+4]
   b) Explain the operation of 4 bit serial in serial out (SISO) register with timing diagram. [5]
7. Explain the operation of 3 bit Asynchronous up/down counter with timing diagram. [6]
8. Design a synchronous sequential machine such that it gives output Z = 1 if input contains the message 110 and it retains in its own state for other condition giving output zero. Use J-K Flip-Flop. [10]
9. What do you mean by static and dynamic hazards? Give example of static hazards and explain how do you eliminate such hazards? [4+2]
10. With the help of block diagram explain the operation of frequency counter. [4]
11. Draw the schematic diagram of TTL NOR gate and explain about totem pole. [6]

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17 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2075 Ashwin

Exam.	Back		
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Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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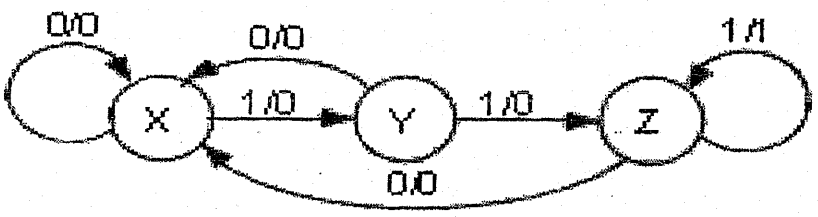
1. Describe in your own words the characteristics of an analog and a digital signal. Convert A2.64H into its octal and decimal equivalents. [2+4]
2. Explain BCD code with suitable examples. [5]
3. Simplify the function using K-map $F=\sum(0, 1, 4, 8, 10, 11, 12)$ and $D=\sum(2, 3, 6, 9, 15)$. Also realize the simplified circuit using NOR Gates. [4+2]
4. Explain the operation of octal to binary encoder with necessary diagrams. Convert A+B'C in to canonical form. [3+3]
5. Describe the importance of parity bits in communication system. Explain 3 bits odd parity generator circuit clearly. [3+3]
6. Realize the circuit diagram for BCD decoder. Explain 1's and 2's complements with examples? [3+3]
7. Explain the operation of edge triggered S-R Flip-Flop with timing diagram and truth table. [6]
8. Design half subtractor circuit using HDL. [4]
9. Define synchronous sequential circuits. Explain the operation of asynchronous mod-12 counter with necessary diagrams. [1+5]
10. Design a synchronous sequential machine from the state diagram given below. Use S-R Flip-Flop. [10]



11. Explain the operation of 4 bit serial in parallel out (SIPO) register with timing diagram. [4]
12. What is the role of hazards in asynchronous circuit design? Explain two bit magnitude comparator with necessary diagrams. [2+4]
13. Draw the schematic diagram of TTL NAND gate and explain about the transistor switch. [2+3]
14. With the help of block diagram explain the operation of Time measuring circuit. [4]

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27 TRIBHUVAN UNIVERSIT

INSTITUTE OF ENGINEERING

Examination Control Division

2073 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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1. a) Define the positive logic and negative logic with examples. [2]

   b) Prove that NOR Gate is an universal gate. Realize EX-OR gate using only NAND gate. [6]

2. Convert the decimal number 73 into gray code and perform the addition (-5+13) by using 2's complement method. [2+3]

3. Simplify the following function using K-map and implement the result using suitable gates. [4+2]

   $F(A,B,C,D) = \Sigma m\,(7,9,12,13,14,15) + d\,(0,2,3,5)$

4. a) Design a circuit that compares two 4-bit numbers, A and B, to check if they are equal. The circuit has one output x, so that x = 1 if A = B and x = 0 if A≠ B. [5]

   b) Implement the following function with a Multiplexer: [4]

   $F(A,B,C,D) = \Sigma\,(0,1,3,4,8,9,15)$

5. Define Flip-Flop. Explain the operation of positive edge trigger J-k Flip Flop with excitation table. Also derive its characteristic equation and draw state diagram. [1+3+2+2]

6. What is the difference between Asynchronous and Synchronous counter? Design Mod-13 synchronous counter using J-K flip flop and also draw its timing diagram. [2+6]

7. Explain the different types of registers with suitable block diagram. [3]

8. Explain the operation of 4-bit serial in serial out (SISO) shift left register with timing diagram. [6]

9. Design a synchronous sequential machine such that it gives output Z = 1 if it detects input message 011. Use D-Flip-Flop. [10]

10. What do you mean by static and dynamic hazards? Give example of static hazards and explain how do you eliminate such hazards? [2+4]

11. Draw the schematic diagram of TTL NAND gate and explain the propagation delay time. [6]

12. With the help of block diagram, explain the operation of digital frequency counter. [5]

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27 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2074 Ashwin

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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1. a) Explain digital wave form based on TTL compatible logic. (Both for input and output) [3]
   b) What is the importance of De-morgan's laws? Show how a two-input NOR gate can be constructed from a two-input NAND gate. [4]
2. Convert decimal 39 into binary and hexadecimal. Use 2'S complement method to perform the following addition (-28+17) [2+3]
3. Simplify the function using K-map $F = \sum(0,1,4,8,10,11,12)$ and $D = \sum(2,3,6,9,15)$. Also realize the simplified logic circuit. [6]
4. a) What is an encoder? Draw the logic circuit of an encoder that converts Octal number into binary. [1+4]
   b) What is a multiplexer tree? Design the 16 to 1 multiplexer using 4 to 1 multiplexer. [1+4]
5. What is the Setup time and hold time of a flip-flop? With the help of excitation table and K-map, convert R-S flip flop into D and J-K flip flops. [2+6]
6. Describe the operation of 4 bit serial in Serial Out shift register, with timing diagram. Consider the input 1011 to be entered into the register. [6]
7. List the advantages and disadvantages of a synchronous counter over asynchronous counter. Design a 3 bit synchronous counter which follow gray code sequence. [2+6]
8. Design a sequential machine that produces output Y = 1 when it detects the serial input X = 100. [10]
9. Define fan-in and fan-out with reference to TTL. With a circuit diagram explain the operation of 2-bit TTL NAND gate. [2+6]
10. Draw the block diagram with decoders to show hour, minute and second. [6]
11. Write short notes on: (any two) [2×3]
    i) Static and dynamic hazzard
    ii) ROM
    iii) DE-MUX tree

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01 | 13

27 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2072 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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1. Perform the following as indicated in the brackets: [2×4]
   a. $(10.0101)_2 = (?)_{16}$
   b. $(101001001)_{binary} = (?)_{Gray}$
   c. $(93)_{10} = (?)_{Excess\text{-}3}$
   d. $(10.001)_2 - (11.101)_2$ using ***2's complement method.***
2. a) Describe commutative and associative laws of Boolean algebra with examples and simplify A+A'B=A+B. [2+2]
   b) Implement Excusive OR gate by using NAND gates only. [4]
3. Simplify $\sum 1,2,3,8,9,10,11,13,14 + d(0,4,7,12)$ by using K-Map and write its standard product of sum (POS) expression. [4+3]
4. How do you design 32:1 Mux by using multiplexer tree? Implement logic function $Y = \sum m(0,1,3,8,9,13,15)$ by using suitable multiplexer. [4+3]
5. Realize a full-subtractor using suitable demultiplexer and standard getes. [6]
6. Design a simplest logic circuit for 'b' segment of the BCD to 7 segment decoder. [7]
7. Design and draw the circuit diagram of a 3 bit gray code synchronous counter. [7]
8. Draw ripple decade counter and sketch its timing diagram. [5+2]
9. Draw 2-input TTL NAND gate and explain its working principle. [5]
10. How does second section of a digital clock work? Explain its working principle using block diagram. [6]
11. Design a sequential machine that has a single input 'x' and single output 'z'. The machine is required to give high output when it detects the serial sequence of 011 message. Use JK flip-flops only. [12]

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073/4/A

24 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2073 Shrawan

Exam.	New Back (2066 & Later Batch)		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

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1. a) Perform the following code conversions. [3+2]
   i) $(1110)_{gray} = (?)_{BCD}$
   ii) $(1430)_{10} = (?)_{Excess-3}$
   b) Construct two input XOR gate using minimum number of 2-input NAND gates only. [5]
2. Implement a full adder circuit using 4:1 Multiplexers. [5]
3. Draw the circuit diagram and explain the working principle of 4-bit parallel in serial out (PISO) shift register. [7]
4. Simplify $\sum 1,2,3,8,10,13 + d(0,4,5,6,7,9,12)$ by using K-Map and write its standard SOP expression. [6]
5. Design 1:32 dimultiplexer tree using 1:8 DEMUXS and 1:2 DEMUXS only. [6]
6. Draw the schematic diagram of TTL Inverter. Explain the working principle of circuit. [3+4]
7. Derive characteristic equation of a JK flip flop. How do you make it a toggle flip flop? Draw the input and output wave form of JK flip flop. [3+2+2]
8. Differentiate between combinational and sequential circuits. Explain BCD-to-Decimal decoder circuit with suitable diagram. [2+6]
9. Design a synchronous MOD-5 counter along with block diagram and timing diagrams. Also write the applications of counters and shift registers. [6]
10. Sketch block diagram of digital frequency counter and describe its operation. [8]
11. A sequential machine has to detect serial input sequance of 101, the machine output will be high. The machine contains two JK flip flops, A and B. Assume: single input, x and single output Y. [12]

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2/28

27 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2071 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

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1. What is weighted code and non-weighted code? What will be the BCD, Excess-3 and Gray code for the decimal number 15? [2+3]
2. Perform the following addition using 2's complement -5+12 [4]
3. Implement Exclusive OR gate by using NAND gates only. [3]
4. Simplify the following function using K-map and implement the result using only NOR gates. [4+3]

   $F(A, B, C,D) = \sum m (0, 2, 3, 5, 6, 8, 9) + d (10, 11, 12, 13, 14, 15)$
5. Design a 32:1 MUX using only 8:1 MUX. Use block diagrams. [5]
6. Design a combinational logic circuit with 3 input variables that will produce logic high output when more than one input variables are logic low. [4]
7. Show with design that a full-adder can be implemented using two half-adders. Subtract $(16)_{10}$ from $(14)_{10}$ using 2's complement method. [6+2]
8. Derive characteristic equation of a JK flip flop. How do you make it a toggle flip flop? Draw the input and output wave form of JK flip flop. [3+2+2]
9. What is a Shift Register? What are its various types? List out some applications of Shift Register. [5]
10. Differentiate between synchronous and asynchronous counters. Describe the operation of asynchronous 3-bit binary down counter. [2+6]
11. Design a sequential circuit with two D flip flops and two inputs, P and Q. If P = 0, the circuit remains in the same state regardless of the value of Q. When P = 1 and Q = 1, the circuit goes through the state transitions from 00 to 01 to 10 back to 00, and repeats. When P = 1 and Q = 0, the circuit goes through the state transitions from 00 to 10 to 01 back to 00, and repeats. The circuit is to be designed by treating the unused state (s) as don't care condition(s). [12]
12. Discuss the following TTL parameters: [2×4]
    i) Propagation delay
    ii) Worst-Case input voltages
    iii) Fan-out
    iv) Power dissipation
13. Explain clearly the operation of frequency counter with necessary block diagram and timing diagrams. [4]

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7/21 morning

27 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2072 Kartik

Exam.	New Back (2066 & Later Batch)		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
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Subject: - Digital Logic *(EX502)*

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1. What are the major difference between Binary code and BCD code? [2]
2. Explain the operation of gated D flip-flop with timing diagram and truth table. [4]
3. What are the major differences between asynchronous and synchronous counter? Design a Mod-6 synchronous up binary counter using S-R flip flops and draw its timing diagram. [2+6]
4. What are the applications of shift registers? Explain any one of the application with working circuit diagram. [6]
5. Construct MOD-12 asynchronous up-counter with negative edge triggering system in clock. [5]
6. Draw the circuit diagram for 2-input CMOS NAND gate. What is Totem pole output? Explain. [3+3]
7. Convert the decimal number 168 into hexadecimal and gray code by first converting it into binary and perform the following addition using 2's complement 11+15 [2+2+3]
8. Write the minterms of ACD+AB and simplify $\sum 1,2,3,8,9,10,11,13,14+d(0,4,12)$ by using K-Map and write its standard product of sum (POS) expression. [4+6]
9. Differentiate between synchronous and asynchronous inputs of a flip flop with suitable diagram. Derive characteristic equation of a JK flip flop. How do you make it a toggle flip flop? Explain with diagram. [3+5]
10. Draw the schematic diagram of TTL NOR gate. Explain the operation of CMOS to TTL interface. [2+2]
11. Explain with block diagram to build the digital watch from a power supply system. Show second, minute and hour display using decoder. [8]
12. Suppose you have given the following word specification describing the sequential operation of some machine. This machine has a control input X and the clock and two state variables A and B and one output. If the input, is high the machine will change state otherwise this machine is supposed to hold its present state. It also gives output when the sequence is 101. Derive state table and state diagram. Use only T flip-flops and necessary logic gates. [4+8]

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24RE TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
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2070 Chaitra

Exam.	Regular		
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Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
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1. Define digital signal and explain Gray code with example. [1+5]
2. Prove that positive X-OR is equivalent to negative X-NOR. [5]
3. a) Convert the following term into standard min term. A+B'C. [3]
   b) Use K-map method to implement the following function and also draw the reduced circuit using NOR gate. [5]

   $F(A, B, C, D) = \Sigma_m (0, 2, 4, 6, 8, 10, 15)$ and

   $d = \Sigma_m (3, 11, 14)$
4. a) Realize the logic circuit of the following using 8:1 MUX. [4]

   $F(W, X, Y, Z) = \Sigma_m (1, 2, 5, 7, 8, 10, 12, 13, 15)$

   b) When FF_H is ANDed with CO_H what will be the resulting number? Subtract (26) 10 from (16) 10 using 2's complement binary method. [2+2]
5. a) Differentiate between level and Edge triggering? [3]
   b) Explain the operation of two bit magnitude comparator with truth table and circuit diagram. [5]
6. a) Describe different types of registers with diagram. [8]
   b) Illustrate how 1011 data can be stored and retrieve in parallel in serial out shift register with neat timing diagram and truth table. [8]
7. Differentiate synchronous and asynchronous sequential circuits. Explain the operation of mod-12 synchronous counter with timing diagram. [2+6]
8. a) Define state diagram and state table with example. [2]
   b) Design a sequential machine that has one serial input and one output z. The machine is required to give an output z = 1 when the input X contains the message 110. [8]
9. Draw the schematic diagram of TTL two input NOR Gate. [6]
10. Explain briefly the block diagram of an instrument to measure frequency. [5]

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24 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2071 Shawan

Exam.	New Back (2066 & Later Batch)		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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1. Define digital operations. What is Excess-3 Code explain with example. [2+4]
2. Define universal Gate with example. Realise Ex-OR Gate using NAND gate only. [1+4]
3. Simplify the following using K-map and realize the simplified result with NAND gates only. [3+3]
   $$\sum_m(2,5,7,8,10,13) + d(0,6,14,15)$$
4. Implement following combinational circuit with multiplexer. [4]
   $$F(A,B,C,D) = \sum_m(1,3,4,11,12,13,14,15)$$
5. Using seven segment display decoder realize the logic circuit for segment 'b', 'c' and'd'. [5]
6. With neat and clean diagram explain the operation of adder-subtractor circuit. [4]
7. Explain the operation of positive edge triggered RS flip-flop with circuit diagram, trust table and excitation table. [2+8]
8. With clear circuit and timing diagram, explain the operation of parallel in Serial out shift register. [8]
9. Design Synchronous MOD-12 counter using T-flip-flop. [8]
10. Design a sequential machine that can go through 2-bit gray code combination of states. The machine changes its state when serial input is one and remains in same state when input is zero. The machine produces output one when it passes through all states and finally goes back to initial state. (use JK flip flop) [10]
11. What are the characteristics of TTL circuit for logic high and low level? Explain the operation of TTL NAND gate. [2+6]
12. Describe the operation of Digital Clock with block diagram. [6]

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25 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2069 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Define digital IC signal levels. What is Gray Code? Explain with example. [3+3]
2. Construct the given Boolean function: F = (A+B) (C+D) E using NOR gates only. [4]
3. Simplify F (A,B,C,D) = π (0,2,5,8,10) + d(7,15). Write its standard SOP and implement the simplified circuit using NOR gates only. [4+4]
4. a) What is priority Encoder? Design octal to binary priority encoder. [2+4]
   b) Design a 2 bit magnitude comparator. [4]
5. Design a combinational logic that performs multiplication between two 4 bit numbers using binary parallel adder and other gates. [8]
6. Draw the circuit diagram and explain the operation of positive edge triggered JK flip-flop. What are the drawbacks of JK flip-flop? [7+1]
7. Explain the Serial in Serial out (SISO) shift register with timing diagram. [4]
8. Design the synchronous decade counter and also show the timing diagram. [8]
9. Design a sequential machine that detects three consecutive zeros from an input data stream X by making output, Y = 1. [12]
10. Draw the schematic circuit for CMOS NAND gates. What do you mean by totem-pole output? [4+4]
11. Describe the operation of a frequency counter. [4]

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25 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2070 Ashad

Exam.	New Back (2066 & Later Batch)		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. a) What are the different logical operations? Explain. [3]
   b) Explain different coding system used to represent data. [3]
2. Explain the operation of NAND, NOR, XOR and NOT gates with Boolean expression and truth table. [4]
3. Simplify the Boolean function in both SOP and POS and the implement using basic gates only: $F(A, B, C, D) = \sum (0, 1, 3, 4, 8, 9, 15)$ [8]
4. a) Design 8- to -3 line priority encoder. [4]
   b) Design a combinational logic that produces square of 3 bit number using ROM. [6]
5. a) Implement the full adder using two half adders. [3]
   b) Explain the working principle of binary multiplication. [5]
6. Explain the operation of RS flip flop showing it's logic diagram, characteristic table and then derive its characteristics equation and excitation table. [8]
7. With clear circuit diagram, explain the operation of parallel in-Serial out shift register. [4]
8. What do you mean by Presettable Counter? Design a modulo - 12 counter using T-Flip flop. [1+7]
9. Design a sequential machine that takes the one bit of serial data x as input and gives the one bit of data as output z. The machine gives an output z = 1 when the input sequence of x contains the message 0100. [12]
10. What are the parameters of TTL? Explain the operation of 74C00 CMOS. [2+6]
11. Explain the operation of digital clock with neat and clean diagram. [4]

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25 TRIBHUVAN UNIVERSITY

INSTITUTE OF ENGINEERING

Examination Control Division

2068 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX 502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. List out the name of universal gates and why they are called universal gate? Relise Ex-OR Gate using only NAND gates. [2+2]
2. Explain Excess 3 code with suitable examples. [6]
3. Simplify the function using K-map F= $\sum(0,1,4,8,10,11,12)$ and D = $\sum(2,3,6,9,15)$. Also convert the result into standard minterm. [3+5]
4. Design a 32 to 1 multiplexer using 16 to 1 and 2 to 1 multiplexers. [5]
5. Design a 3-bit even parity generator and 4-bit even parity checker circuit. [5]
6. Draw the block diagram of n-bit full adder and explain its operation. [8]
7. Write down the drawbacks of SR flip flop. Explain the operation of data flip flop with timing diagram and truth table. [1+7]
8. With clear circuit and timing diagram, explain the operation of Serial in - Serial out shift register. [4]
9. Define ripple counter. Explain the operation of mode-10 ripple counter with timing diagram. [1+7]
10. Design a sequential machine that has one serial input and one output z. The machine is required to give an output z = 1 when the input x contains the message 1010. [12]
11. Describe the voltage profile of TTL. Explain the operation of TTL to CMOS interface. [2+6]
12. What is frequency counter? Explain with block diagram. [4]

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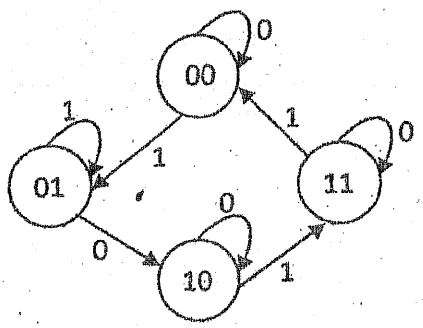
25 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2069 Ashad

Exam.	New Back (2066 & Later Batch)		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic *(EX 502)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Describe in your own words the characteristics of an analog signal and a digital signal. [3]
2. Define positive and negative logic with examples [3]
3. Construct the basic gates using only universal gates. [4]
4. Simplify the following using K-map. $\sum_m(3,4,6,8,10,15) + d(0,2,7,14)$. [3]
5. What are the static hazards in combinational circuit? Also explain how these hazards can be covered. [5]
6. Explain the operation of BCD to decimal decoder with truth table and circuit diagram. Implement 1:4 demux using VHDL. [6+4]
7. Design a full adder circuit using HDL. [4]
8. What is a Fast Adder? Explain with examples. [4]
9. Draw the circuit diagram and explain the operation of edge triggered RS flip-flop. Convert RS flip-flop to JK flip-flop. [5+3]
10. Explain the working of serial in -serial out register clearly. [4]
11. Differentiate between the synchronous and Asynchronous counter. Draw and explain the operation of Asynchronous Decade counter with clear timing diagram. [2+6]
12. Design Synchronous sequential circuit for the given state diagram using JK flip flop. [12]



13. Draw the schematic diagram of TTL NAND gate and explain about the CMOS characteristics. [2+6]
14. With the help of block diagram explain the operation of frequency counter. [4]

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INSTITUTE OF ENGINEERING
Examination Control Division
2068 Baishakh

Exam.	Regular / Back		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt All questions.*
- ✓ *The figures in the margin indicate Full Marks.*
- ✓ *Assume suitable data if necessary.*

1. Draw the general input output voltage profile for TTL gates and also mention the noise margin. What do you mean by Gray code? [3+1+2] [7]
2. Why NAND and NOR gates are called Universal gates? Illustrate with examples. [4] [3]
3. What do you mean by HDL? Design a 2 to 4 line decoder circuit using HDL. [2+3]
4. Simplify $\pi(0, 4, 5, 8, 9, 11, 15)$ using K-Map and write its standard SOP expression. [4+2] [8]
5. Draw the circuit of 4 bit RCA (Ripple Carry Adder), using only block diagrams. What are the problems associated with RCA. Explain how these problems can be eliminated. [4+2+2]
6. Draw the schematic diagram of TTL NOR gate. Discuss the characteristics of TTL 74XX series gates. [6] [5] [4]
7. Draw the circuit diagram of edge triggred JK flip flop and explain it. [5]
8. What is a shift register? With clear timing diagram, describe the operation of a 4-bit parallel - in serial - out (PISO) shift register. [2+6] [7]
9. What is a counter? Design a MOD - 6 synchronous counter. Draw its timing diagram. [5]
10. Design a synchronous state machine with the following specification: [12]
    a) No. of input: 1
    b) No. of output: 1
    c) The output of the machine is to be set high when the data in the input is 110 in sequence, starting from the MSB (Use SR flip - flop).
11. With an example, state and explain the problems associated in the design of asynchronous sequential circuit. [6] [2]
12. Design a two bit magnitude comparator. [6] [6]

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[3]

[3]

[7]

24 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2067 Ashadh

Exam.	Regular/Back		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic

- Candidates are required to give their answers in their own words as far as practicable.
- *Attempt All questions.*
- *The figures in the margin indicate Full Marks.*
- *Assume suitable data if necessary.*

1. Convert the following numbers from the given base to the bases indicated: [1×6]
   a) Octal 623.77 to decimal, binary and hexadecimal
   b) Hexadecimal 2AC5.D to decimal, octal and binary

2. Perform the subtraction with the following decimal and binary numbers using 9's and 1's complement respectively. [2+2]
   a) 3570-2100 (Using 9's complement)
   b) 10010-10011 (Using 1's complement)

3. Prove the following Boolean expression: [4+4+2]

$$AB + A\bar{B}C + \bar{A}BC = AB + AC + BC$$

And simplify Σ1,2,3,8,9,10,11,14) and d(0,4,12) by using K-map and write its standard product of sum (POS) expression.

4. Construct a 5×32 decoder using 3 to 8 decoders and standard logic gate if necessary. Define the term 'decoder'. [8]

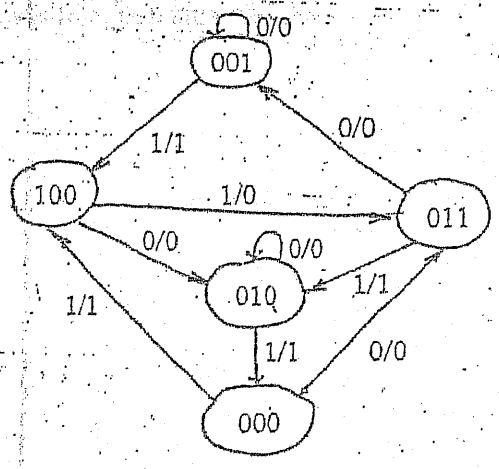
5. State De-Morgan's theorem. Why NAND and NOR gates are called an universal logic gates. [3+6]

6. Explain about JK-flip-flop along with their truth table and characteristic equation. [6]

7. Design a mod-10 synchronous counter showing its state circuit diagram and output waveforms. [6]

8. Describe briefly the operation of a 4-bit serial in-parallel out register with a clear circuit diagram. [5]

9. A sequential circuit has one input and one output. The state diagram is shown in figure. Design the sequential circuit with RS-flip-flops. [10]



10. Explain with wave diagram how can you display a letter E in a CRT under 5×7 matrix format. [6]

11. Write short notes on: (any two) [5×2]
   a) Multiplexing and demultiplexing
   b) Gray code
   c) Fan-in and fan-out, propagation delay
   d) Parity generator

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